Examiner for the courtesy extended during the interview held on May 2, 1991.

As agreed during the interview the above amendments to the specification correct the informality noted by the Examiner in the Office Action with regard to control signals. It was pointed out to the Examiner that the control signals are identified as ϕ_1 ϕ_2. Amendments were made to the specification to further clarify that ϕ_1 and ϕ_2 are control signals. As discussed and agreed during the interview the term "driving ability" concerns the ability of the internal power supply means to drive its load circuits. In other words, the control signal causes the internal supply means to supply more or less current thereby effecting the ability of the internal power supply means to drive its load circuit.

Additional amendments were made to the specification to more clearly describe features of the present invention.

Therefore, the objection to the specification is overcome and should be withdrawn.

An additional copy of Takanashi (U.S. Patent 4,239,980) is provided herewith to be made of record in the present application. Takanashi was discussed during the interview as being prior art. It was pointed out during the interview that the present invention differs from that taught by Takanashi for the following reasons.

The present invention provides reference voltage generating means which generates a reference voltage so that any level of reference voltage can be provided and can in fact be changed

based upon the operation of the circuit. Such a reference voltage generating means is not taught or suggested by Takanashi.

An additional copy of the 1984 IEEE International Solid State Circuits Conference entitled "An Experimental 1Mb DRAM with On-Chip Voltage Limiter" by K. Itoh, et al. is provided herewith.

Further, the Examiner is informed of Applicants desire to incorporate U.S. Patent No. 4,482,985 as a parent to the present Application. Particularly, the Examiner is informed that a Petition under 37 CFR 1.182 will be filed with the Petitions Office in order to obtain relief so as to amend Application Serial No. 562,929 filed on December 19, 1983, now abandoned, to recite in the specification thereof that it is a Continuation-In-Part Application of Application Serial No. 368,162 filed April 14, 1982 which issued as U.S. Patent No. 4,482,985 on November 13, 1984. As you can see Application Serial No. 562,969 filed on December 19, 1983, now abandoned, was co-pending with application Serial No. 368,162 filed on April 14, 1982 which issued as U.S. Patent No. 4,482,985 on November 13, 1984.

Also a Reissue application will be filed on U.S. Patent No. 4,916,389 so as to further claim the priority of U.S. Patent No. 4,482,985 by amending the specification to recite that it is a continuation of Application Serial No. 562,969 filed December 19, 1983, now abandoned, which is a continuation-in-part of Application Serial No. 368,162 filed April 14, 1982 which issued as U.S. Patent 4,482,985 on November 13, 1984.

The present application will be amended to recite the above noted chain of priority once the Petition has been granted.

Various amendments were made throughout claims 7, 9-13 and 15-19 in order to more clearly recite features of the present invention. Also new claims 20-73 were added to claim features of the present invention not taught or suggested by any of the references of record whether taken individually or in combination with each with other. Particularly, new independent claims 20-24 were added to recite the internal power supply means and the reference voltage generating means not taught or suggested by any of the references of record whether taken individually or in combination with each other. Dependent claims 25-73 variously depend from claims 7, 9-13 and 15-24.

The Examiner is respectfully requested to examine new claims 20-73.

The drawings stand objected to due to a misspelled word in Fig. 32. Filed herewith are Proposed Drawing Corrections correcting the misspelled word in Fig. 32. Therefore, this objection is overcome and should be withdrawn.

Claims 7, 9-13 and 15-19 stand rejected under 35 USC 102(b) as being anticipated by Alaspa. This rejection is traversed for the following reasons. Applicants submit that the apparatus of the present invention as now recited in claims 7, 9-13 and 15-73 is not taught or suggested by Alaspa whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Alaspa discloses an on-chip power-on reset circuit which provides a voltage limiter for MOS IC load circuits. Fig. 3 of

Alaspa shows the relationship between an external supply voltage VR and an internal supply voltage VDD. The relationship as defined in Alaspa provides a first rate A, a second rate E, a third rate C and a fourth rate D. The general purpose of the apparatus taught by Alaspa is for a slow VDD voltage to provide an output reset VR which is essentially clamped to the ground for at least part of the power-on time until VDD reaches some value at which time VR abruptly increases along segment C in Fig. 3 to VDD volts and remains equal to VDD volts along segment D as VDD continues to increase. The dotted line segments A and B in Fig. 3 of Alaspa represent possible undesirable variations in the transfer characteristics which could result from parasitic leakage currents at low voltages at various modes of the circuits. Thus as can be seen, Alaspa provides apparatus which attempts to clamp the internal supply voltage at "0" at a power-on reset time interval of the circuit until the external supply voltage reaches a predetermined level.

This operation of Alaspa is entirely different from that of the present invention being that the apparatus taught by Alaspa merely operates in an initial time period after power-on reset of the circuit whereas the present invention provides an internal supply voltage which is set to different rates during operation of the apparatus not necessarily the initial power-on interval. Thus, Alaspa does not provide apparatus which causes an internal supply voltage to increase at different rates throughout the normal operation range of a circuit. Alaspa instead merely provides apparatus which clamps the supply voltage at "0" until

the supply voltage reaches a predetermined level during power-on reset interval. In Alaspa once the external supply voltage reaches a predetermined level the internal supply voltage is allowed to increase at the same rate as the external supply voltage. The present invention does not operate in this manner.

Therefore, the plurality of rates taught in the claims of the present application are not taught by Alaspa particularly being that Alaspa merely clamps the supply voltage to "0" until a predetermined level is reached and then allows the internal supply voltage to increase at the same rate as the external supply voltage.

Therefore, Alaspa does not teach or suggest when the external supply voltage is not higher than a predetermined first voltage, the internal supply voltage of the internal power supply means increases at a first rate which is substantially equal to the increasing rate of the external supply voltage when the external supply voltage is between a level exceeding the first voltage and predetermined second voltage the internal supply voltage increases at a second rate which is lower than the increasing rate of the external supply voltage and after the external supply voltage exceeds the second voltage, the internal supply voltage increases at a third rate which is higher than the second rate as recited in the claims of the present application.

Further, provided in the apparatus of the present invention is a control signal which controls the driving ability of the internal power supply means. Alaspa does not teach or suggest such apparatus as recited in the claims of the present

application. Alaspa merely provides a circuit which clamps the internal supply voltage to "0" until the external supply voltage reaches a predetermined level. There is no teaching that the circuit as taught by Alaspa receives a control signal which controls the driving ability thereof as in the present invention.

Therefore, Alaspa does not teach or suggest that the first circuits are fed the internal supply voltage, the internal power supply means is fed a control signal and wherein a driving ability of the internal power supply means is controlled by the control signal as recited in the claims of the present application.

A further difference between the present invention and the apparatus taught by Alaspa is that the first circuit in the present invention is fed the internal supply voltage whereas in Alaspa no such first circuit is recited.

With respect to new claims 20-73 Alaspa does not teach or suggest the internal power supply means and the reference voltage generating means as recited therein.

Therefore, Applicants submit that the apparatus of the present invention as now recited in claims 7, 9-13 and 15-73 is not taught or suggested by Alaspa whether taken individually or in combination with any of the other references of record.

Claims 7, 9-13 and 15-19 stand rejected under 35 USC 102(b) as being anticipated by Suzuki. This rejection is traversed for the following reasons. Applicants submit that the apparatus of the present invention as now recited in claims 7, 9-13 and 15-73 is not taught or suggested by Suzuki whether taken individually

or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Suzuki, very similar to Alaspa, discloses an on-chip power-on reset circuit implemented by bipolar technology. Fig. 2 of Suzuki discloses the operation of the circuit taught therein which is very similar to that taught in Alaspa. Therefore, the same arguments presented above with respect to the use of Alaspa to reject the claims of the present application apply as well to the use of Suzuki to reject the claims of the present application.

Particularly, Applicants note that Suzuki as with Alaspa teaches an apparatus which operates during the power-on reset interval of a circuit. The apparatus taught by Suzuki attempts to maintain the internal supply voltage being supplied to a circuit to "0" level during the initial reset interval until the external supply voltage reaches a predetermined level. Suzuki also provides a pulse signal during the initial power-on reset period so as to reset other circuits during this interval. As with Alaspa, Suzuki does not teach or suggest apparatus which operates or limits the voltage during normal operation of the circuit being that in Suzuki as in Alaspa once the external supply voltage reaches a predetermined level then the internal supply voltage is allowed to increase or decrease at the same rate and level as the external supply voltage.

In the present invention various rates of increase and decrease of the internal supply voltage is caused during the

normal operation of the circuit based upon the level of the external supply voltage. Such a feature is not taught by Suzuki.

Therefore, Suzuki does not teach that when the external supply voltage is not higher than a predetermined first voltage, the internal supply voltage of the internal power supply means increases at a first rate which is substantially equal to the increasing rate of the external supply voltage, when the external supply voltage is between a level exceeding the first voltage and predetermined second voltage, the interim supply voltage increases at a second rate which is lower than the increasing rate of the external supply voltage and after the external supply voltage exceeds the second voltage, the internal supply voltage increases at a third rate which is higher than the second rate as recited in the claims of the present application.

Further, Suzuki fails to teach or suggest that the internal power supply means is fed a control signal and the driving ability of the internal power supply means is controlled by the control signal as recited in the claims of the present application.

Still further, with respect to claims 20-73 Suzuki fails to teach or suggest internal power supply means and reference voltage generating means as recited therein.

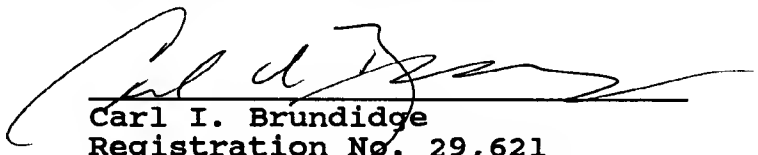
Therefore, Applicants submit that the apparatus of the present invention as now recited in claims 7, 9-13 and 15-73 of the present application and allowable over the prior art of record.

The remaining references of record have been studied. Applicants submit that they do not supply the deficiencies noted above with respect the references utilized in the rejection of claims 7, 9-13 and 15-19

In view of the foregoing amendments and remarks, Applicants submit that claims 7, 9-13 and 15-73 are in condition for allowance. Accordingly, early allowance of claims 7, 9-13 and 15-73 is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 501.20699VC1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,



Carl I. Brundidge
Registration No. 29,621
ANTONELLI, TERRY, STOUT & KRAUS

CIB/hpg
(202) 828-0300

ISSCC 84 / FRIDAY, FEBRUARY 24, 1984 / CONTINENTAL 5-9 / FAM 18.6

Ref. 3

SESSION XVIII: 256K/1Mb DRAMS II

FAM 18.6: An Experimental 1Mb DRAM with On-Chip Voltage Limiter

Kiyoo Itoh, Ryoichi Hori, Jun Etoh, Shojiro Asai, Norikazu Hashimoto, Kunihiro Yagi, Hideo Sunami

Hitachi Central Research Laboratory

Tokyo, Japan

THIS PAPER WILL DESCRIBE an experimental 21μm^2 cell, single 5V, 1Mb NMOS DRAM with an on-chip voltage limiter, a typical access time of 90ns, typical power dissipation of 300mW at 260ns cycle time and 46mm^2 chip area.

The key to achieving 1Mb is the higher signal-to-noise ratio, while maintaining single 5V operation, even for small feature size MOSTs. To meet this requirement, three developments are proposed: a Corrugated Capacitor (memory) Cell (CCC)[1], a sensing method, and an on-chip voltage limiter[1]. The results would include about a 2.2-times signal-to-noise ratio improvement and provision for single 3V operation.

The memory cell that combines CCC and a folded data line arrangement is illustrated in Figure 1. The cell measures 3x7μm^2 and has a cell storage capacitance, C_s, of 60fF due to the CCC structure, which is about 7.5 times as large as a conventional one.

Figure 2 shows the sensing design. A small data line capacitance, C_D, can be obtained using a multi-divided data (sense) line structure without any additional column decoders, as would be needed in a conventional scheme. That is, the column decoder output signal, ϕ_Y, which consists of the second level Al wire and runs along the data line, can control each data-I/O switch, SW. This can reduce C_D by about one third, assuming a given chip area and the 16-division data line organization shown in Figure 2. The resultant C_D is 290fF. Thus, a large cell signal can be obtained.

Figure 3 shows a limiter circuit for application to the memory array and its associated circuitries. This circuit configuration permits single 5V operation. MOSTs, with gate length, L_g, of 2.4μm and gate oxide thickness, t_{ox}, of 40nm are used in the peripheral circuitry, which contributes less to chip size, so as to operate directly with the external supply voltage, V_{cc}. On the other hand, small MOSTs (L_g = 1.6μm, t_{ox} = 20nm) are used in the memory array and its associated circuitry, which are the main determinants of chip size, so as to realize high density. However, these small MOST circuits must be operated based on a lower voltage limiter. Note that the precharged data line and the word-line voltages are V_L and $V_L + V_T$ (V_T: threshold voltage), respectively.

Figure 4 shows the experimental V_L characteristics. To ensure long term reliability of the small MOSTs, V_L was chosen to be 3.7V at the nominal V_{cc} of 5V. This V_L is set by the conductance ratio of Q_1 and Q_2. To eliminate a race problem at V_{cc} above 5V, an additional ΔV_L is provided by Q_3, Q_4 and Q_5. This results in a wide V_{cc} margin.

A microphotograph of the 1Mb RAM using low resistive and poly Si gates is shown in Figure 5. This chip measures 4.67 x 9.86mm^2, which permits assembly in a standard 300mil 18 pin DIP. Waveforms for a typical chip, having a typical access time from $\overline{RAS}$ low of 90ns, are shown in Figure 6. Power dissipations at nominal operating condition (5V, 25°C) are 300mW at 260ns cycle time and 10mW, respectively. Table 1 summarizes the ORAM features.

Acknowledgments

The authors would like to thank M. Kubo and K. Sato for their constant encouragement during the course of this work.

Technology	low resistive/poly-Si gate N-MOS 2 level Al wiring
Cell Size	3μm x 7μm (21μm^2)
Chip Size	4.67mm x 9.86mm (46mm^2)
Access Time	90ns (5V, 25°C)
Cycle Time	260ns (5V, 25°C)
Power Supply	5V ± 10%
Active Current	60mA (5V, 25°C, 260ns cycle)
Standby Current	2mA (5V, 25°C)
Refresh	512 cycles at 8ms intervals
Interface	TTL compatible
Package	18pin, 300-mil DIP

TABLE 1–Features of ORAM.

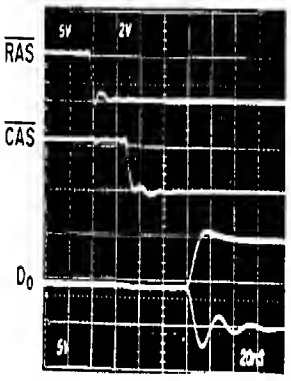


FIGURE 6–Operating waveforms for 1Mb RAM: V_{cc} = 5V, 25°C loading capacitance of D_O is 100pF.

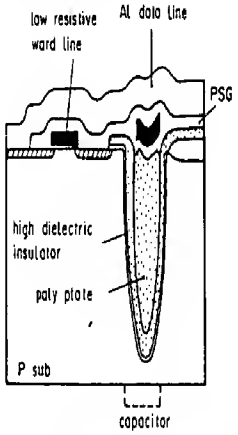


FIGURE 1–CCC memory cell cross section.

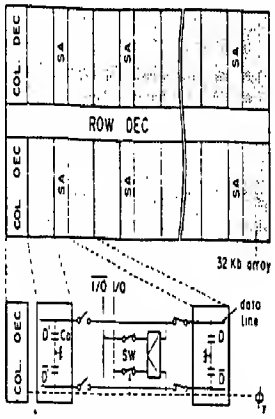


FIGURE 2–Memory array organization for 1Mb chip. SA denotes sense amplifier.

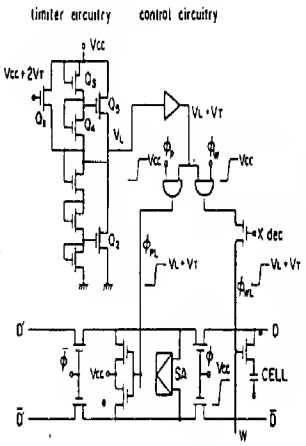


FIGURE 3–Limiter circuitry with application to a memory array and its associated circuitry: ϕ_P, ϕ_{PL} – precharge and limited precharge clock; ϕ_W, ϕ_{WL} – word and limited word clock; D, $\overline{D}$, D', $\overline{D}'$ – data line, ϕ, $\bar{\phi}$ – data line selection clock.

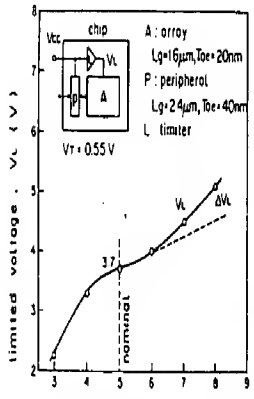


FIGURE 4–Experimental V_L characteristics.

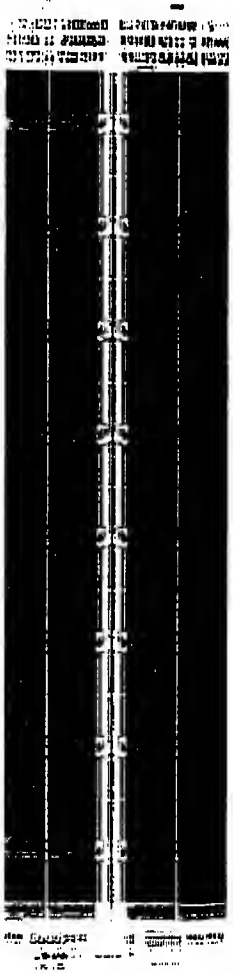


FIGURE 5–Microphotograph of 1Mb chip.

[1] Sunami, H., et. al., "A Corrugated Capacitor Cell (CCC) for Megabit Dynamic MOS Memories", IEDM abs. No. 26.9: 1982.

[2] Mano, T., et. al., "Submicron VLSI Memory Circuits", ISSCC DIGEST OF TECHNICAL PAPERS, p. 234: Feb., 1983.

0193-6530/84/0000-0282$01.00 © 1984 IEEE